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| EXAMINER | |
|---|---|
| PRENTY, MARK V | |

| ART UNIT | PAPER NUMBER |
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| 2822 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/538,217 | HIJZEN, ERWIN A | |
| | Examiner | Art Unit | |
| | MARK PRENTY | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,8-11 and 13-16* is/are rejected.

7)☒ Claim(s) *2,3,7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

This Office Action is in response to the response filed on December 21, 2007.

Claim 2 is objected to because "the step of etching the trench" lacks antecedent basis and should read, "the step of forming the trench."

Claim 3 is objected to because "etching away the oxide formed on the side wall oxide" and "the gate oxide" should read, "etching away the oxide formed on the sidewalls" and "a gate oxide," respectively.

Claims 1, 4, 6, 9, 10, 11, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 4,541,001 to Schutten et al. (Schutten '001).

As to independent claim 1, Schutten '001 discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Figs. 2-6 disclosure) comprising the steps of: providing a silicon device body 4/8 having a first major surface, the silicon device body having a drain region 4 of a first conductivity type and a body region 8 over the drain region; forming a trench 12 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; etching the silicon at the base of the trench to form porous silicon 18 at the base of the trench (see column 7, lines 30-37); and thermally oxidizing the device to oxidize the porous silicon at the bottom of the trench to form a plug at the base of the trench (see column 7, lines 40-42); and depositing conductive material within the trench to form a gate 34.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 4, Schutten '001's step of forming the trench 12 includes providing a mask 117 on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening.

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 6, Schutten 001's step of etching the silicon at the bottom of the trench 12 to form porous silicon 18 includes dry-etching the bottom of the trench through the same mask 117 used to define the trench (see column 7, lines 22-37).

Claim 6 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 9, Schutten '001 discloses a trench MOSFET (see the entire patent, including the Fig. 6 disclosure) comprising: a drain region 4 of first conductivity type; a body region 8 over the drain region; a trench 12 extending from a first major surface through the body region; source regions 10 of the first conductivity type laterally adjacent to the trench at the first major surface; thermal gate oxide 30 and 32 on the sidewalls of the trench; a gate electrode 34 or 36 in the trench insulated from the body region by the gate oxide; characterized by a thick oxide plug formed of oxidized porous silicon 18 (see column 7, lines 30-42) at the base of the trench extending into the drain region.

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 10, Schutten '001's body region 8 is of second conductivity type opposite to the first conductivity type.

Claim 10 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to independent claim 11, Schutten '001 discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Figs. 2-6 disclosure), the method comprising: providing a silicon device body 4/8 having a first major surface, the silicon device body having a drain region 4 of a first conductivity type and a body region 8 over the drain region; forming a trench 12 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; etching the silicon at the base of the trench to form porous silicon at the base of the trench (see column 7, lines 30-37); thermally oxidizing the device to oxidize the porous silicon at the base of the trench to form a plug at the base of the trench (see column 7, lines 40-42), wherein thermally oxidizing the device forms sidewall oxide 30 and 32 on the sidewalls of the trench; and depositing conductive material within the trench to form a gate 34 or 36.

Claim 11 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 13, Schutten 001's step of forming the trench 12 includes providing a mask 117 having an opening and on the first major surface and etching through the opening.

Claim 13 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

As to dependent claim 15, Schutten 001's step of etching the silicon at the bottom of the trench 12 to form porous silicon 18 includes dry-etching the base of the trench through the same mask 117 used to define the trench (see column 7, lines 22-37).

Claim 15 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '001.

Claims 1, 4-6, 9-11 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 4,612,465 to Schutten et al. (Schutten '465).

As to independent claim 1, Schutten '465 discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Figs. 14-20 disclosure) comprising the steps of: providing a silicon device body 202/204 having a first major surface, the silicon device body having a drain region 202 of a first conductivity type and a body region 204 over the drain region; forming a trench 226 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base (see the Fig. 18 disclosure); etching the silicon at the base of the trench to form porous silicon 228 at the base of the trench (see column 10, lines 31-40); and thermally oxidizing the device to oxidize the porous silicon at the bottom of the trench to form a plug at the base of the trench (see column 10, lines 44-46); and depositing conductive material within the trench to form a gate 238.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 4, Schutten '465's step of forming the trench 226 includes providing a mask 222/224 on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening.

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 5, Schutten '465's mask 222/224 comprises oxide 222.

Claim 5 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 6, Schutten '465's step of etching the silicon at the bottom of the trench 226 to form porous silicon 228 includes dry-etching the bottom of the trench through the same mask 222/224 used to define the trench (see column 10, lines 25-40).

Claim 6 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 9, Schutten '465 discloses a trench MOSFET (see the entire patent, including the Fig. 20 disclosure) comprising: a drain region 202 of first conductivity type; a body region 204 over the drain region; a trench 226 extending from a first major surface through the body region; source regions 214 of the first conductivity type laterally adjacent to the trench at the first major surface; thermal gate oxide 232 on the sidewalls of the trench; a gate electrode 238 in the trench insulated from the body

region by the gate oxide; characterized by a thick oxide plug formed of oxidized porous silicon 228 (see column 10, lines 31-46) at the base of the trench extending into the drain region.

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 10, Schutten '465's body region 204 is of second conductivity type opposite to the first conductivity type.

Claim 10 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to independent claim 11, Schutten '465 discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Figs. 14-20 disclosure), the method comprising: providing a silicon device body 202/204 having a first major surface, the silicon device body having a drain region 202 of a first conductivity type and a body region 204 over the drain region; forming a trench 226 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; etching the silicon at the base of the trench to form porous silicon at the base of the trench (see column 10, lines 31-40); thermally oxidizing the device to oxidize the porous silicon at the base of the trench to form a plug at the base of the trench (see column 10, lines 44-46), wherein thermally oxidizing the device forms sidewall oxide 232/234/236 on the sidewalls of the trench (see column 10, lines 48-54); and depositing conductive material within the trench to form a gate 238.

Claim 11 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 13, Schutten '465's step of forming the trench 226 includes providing a mask 222/224 having an opening and on the first major surface and etching through the opening.

Claim 13 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 14, Schutten '465's mask 222/224 comprises oxide 222.

Claim 14 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

As to dependent claim 15, Schutten '465's step of etching the silicon at the bottom of the trench 226 to form porous silicon 228 includes dry-etching the bottom of the trench through the same mask 222/224 used to define the trench (see column 10, lines 25-40).

Claim 15 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Schutten '465.

Claims 1, 4-6, 8-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,809,375 to Takemori et al. (Takemori) together with United States Patent 4,541,001 to Schutten et al. (Schutten '001).

As to independent claim 1, Takemori discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Fig. 1B and Figs. 5-21 disclosure), comprising: providing a silicon device body 17/18/19 having a first

major surface, the silicon device body having a drain region 17/18 of a first conductivity type and a body region 19 over the drain region; forming a trench 10 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; filling the bottom of the trench with silicon oxide 51 (Fig. 12) to form a plug 16 at the base of the trench; and depositing conductive material within the trench to form a gate 11.

The difference between claim 1 and Takemori is claim 1's silicon oxide plug is formed by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon, while Takemori's silicon oxide plug is formed by filling the bottom of the trench with silicon oxide.

Schutten '001 teaches forming a trench gate semiconductor device's silicon oxide plug either by filling the bottom of the trench with silicon oxide or by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon (see the entire patent, including column 2, lines 1-26, and column 7, lines 30-45).

It would have been obvious to one skilled in the art to form Takemori's silicon oxide plug 16 by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon, instead of by filling the bottom of the trench with silicon oxide, because Schutten '001 teaches forming a trench gate semiconductor device's silicon oxide plug either by filling the bottom of the trench with silicon oxide or by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon.

Claim 1 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 4, Takemori's step of forming the trench includes providing a mask on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening (see column 10, lines 17-22).

Claim 4 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 5, Takemori's mask is an oxide hard mask (see column 10, lines 17-22).

Claim 5 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 6, Schutten '001 discloses that the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom of the trench through the same mask used to define the trench (see column 7, lines 30-45).

Claim 6 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 8, Takemori's method further comprises forming a source implant 21 of the first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate

and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.

Claim 8 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to independent claim 9, Takemori discloses a trench MOSFET (see the entire patent, including the Fig. 1B disclosure, for example) comprising: a drain region 17/18 of a first conductivity type; a body region 19 over the drain region; a trench 10 extending from a first major surface through the body region; source regions 21 of the first conductivity type laterally adjacent to the trench at the first major surface; thermal gate oxide 27 on the side walls of the trench; a gate electrode 11 in the trench insulated from the body region by the gate oxide; characterized by a thick silicon oxide plug 16 formed of silicon oxide fill 51 (Fig. 12) at the base of the trench extending into the drain region.

The difference between claim 9 and Takemori is their thick silicon oxide plugs are formed of oxidized porous silicon and silicon oxide fill, respectively.

Schutten '001 teaches forming a trench MOSFET's silicon oxide plug of silicon oxide fill or oxidized porous silicon (see the entire patent, including column 2, lines 1-26, and column 7, lines 30-45).

It would have been obvious to one skilled in the art to form Takemori's trench MOSFET's thick silicon oxide plug 16 of oxidized porous silicon instead of silicon oxide fill because Schutten '001 teaches forming a trench MOSFET's thick silicon oxide plug of silicon oxide fill or oxidized porous silicon.

Claim 9 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 10, Takemori's body region 19 is of second conductivity type opposite to the first conductivity type.

Claim 10 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to independent claim 11, Takemori discloses a method of manufacturing a trench gate semiconductor device (see the entire patent, including the Fig. 1 and Figs. 5-21 disclosure), comprising: providing a silicon device body 17/18/19 having a first major surface, the silicon device body having a drain region 17/18 of a first conductivity type and a body region 19 over the drain region; forming a trench 10 extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; filling the bottom of the trench with silicon oxide 51 (Fig. 12) to form a plug 16 at the base of the trench; thermally oxidizing the device to form sidewall oxide 52 on the sidewalls of the trench (see the Fig. 13 disclosure); and depositing conductive material within the trench to form a gate 11.

The difference between claim 11 and Takemori is claim 11's silicon oxide plug is formed by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon, while Takemori's silicon oxide plug is formed by filling the bottom of the trench with silicon oxide.

Schutten '001 teaches forming a trench gate semiconductor device's silicon oxide plug either by filling the bottom of the trench with silicon oxide or by etching the silicon

at the base of the trench to make it porous and then thermally oxidizing the porous silicon (see the entire patent, including column 2, lines 1-26, and column 7, lines 30-45).

It would have been obvious to one skilled in the art to form Takemori's silicon oxide plug 16 by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon, instead of by filling the bottom of the trench with silicon oxide, because Schutten '001 teaches forming a trench gate semiconductor device's silicon oxide plug either by filling the bottom of the trench with silicon oxide or by etching the silicon at the base of the trench to make it porous and then thermally oxidizing the porous silicon.

Claim 11 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 13, Takemori's forming the trench includes providing a mask having an opening and on the first major surface and etching through the opening (see column 10, lines 17-22).

Claim 13 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 14, Takemori's mask is an oxide hard mask (see column 10, lines 17-22).

Claim 14 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 15, Schutten '001 discloses that the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom

of the trench through the same mask used to define the trench (see column 7, lines 30-45).

Claim 15 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

As to dependent claim 16, Takemori's method further comprises forming a source implant 21 of the first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.

Claim 16 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Takemori together with Schutten '001.

Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if corrected (see above) and rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest the allowable claims as a whole, including the oxidized porous silicon.

The applicant's arguments are moot in view of the new grounds of rejection.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

/MARK PRENTY/

Primary Examiner, Art Unit 2822

/Zandra V. Smith/

Supervisory Patent Examiner, Art Unit 2822